TJA1051

High-speed CAN transceiver

Rev. 04 — 20 October 2009 | Product data sheet

1. General description

The TJA1051 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed (up to 1 Mbit/s) CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1051 is a up from the TJA1050 high-speed CAN transceiver. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- TJA1051T/3 and TJA1051TK/3 can be interfaced directly to microcontrollers with supply voltages from 3 V to 5 V

These features make the TJA1051 an excellent choice for all types of HS-CAN networks, in nodes that do not require a standby mode with wake-up capability via the bus.

2. Features

2.1 General

- Fully ISO 11898-2 compliant
- Suitable for 12 V and 24 V systems
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- V_{IO} input on TJA1051T/3 and TJA1051TK/3 allows for direct interfacing with 3 V to 5 V microcontrollers (available in SO8 and very small HVSON8 packages respectively)

2.2 Low-power management

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up (zero load)

2.3 Protection

- High ElectroStatic Discharge (ESD) handling capability on the bus pins
- Bus pins protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on pins V_{CC} and V_{IO}
- Thermally protected

founded by Philips

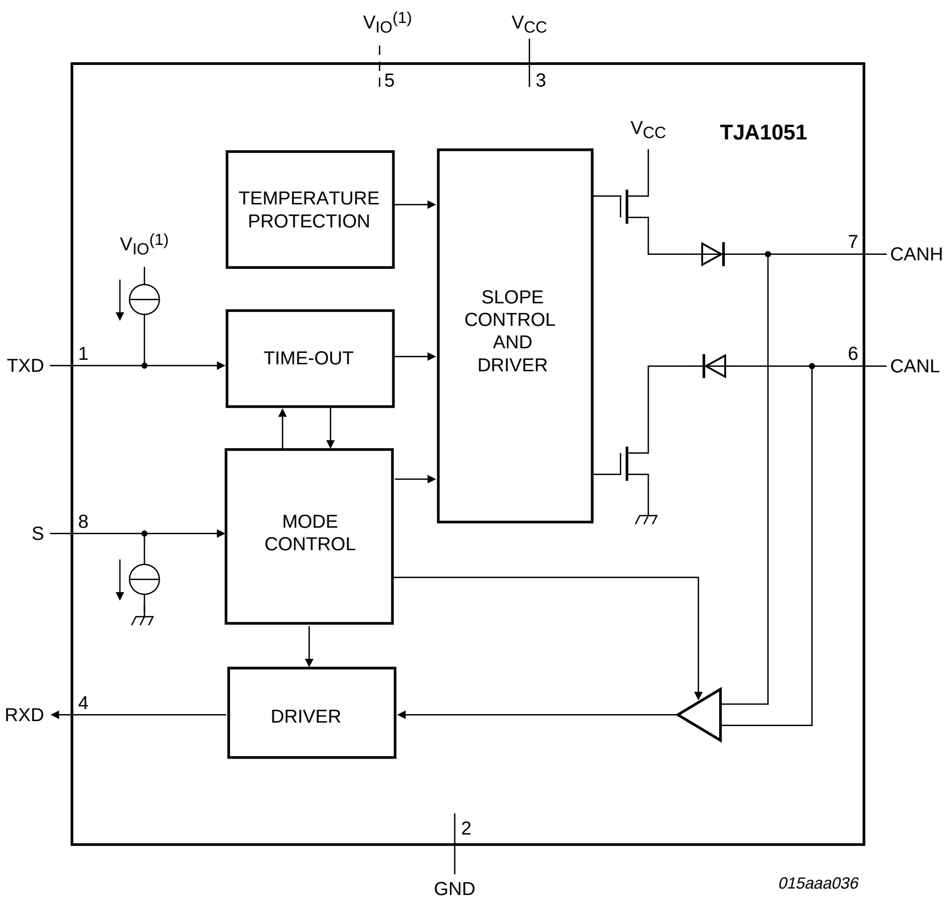
3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1051T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1051T/3[1]	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1051TK/3[1]	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm	SOT782-1

[1] TJA1051T/3 and TJA1051TK/3 with V_{IO} pin.

4. Block diagram



(1) In a transceiver without a V_{IO} pin, the V_{IO} input is internally connected to V_{CC}.

Fig 1. Block diagram

5. Pinning information

5.1 Pinning

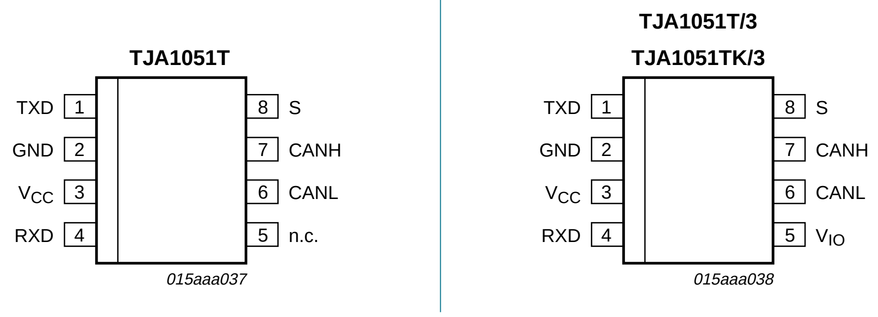


Fig 2. Pin configuration diagrams

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2	ground supply
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines
n.c.	5	not connected; in TJA1051T version only
V_{IO}	5	supply voltage for I/O level adapter; in TJA1051T/3 and TJA1051TK/3 versions only
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
S	8	Silent mode control input

6. Functional description

The TJA1051 is a high-speed CAN stand-alone transceiver with Silent mode. It combines the functionality of the TJA1050 transceiver with improved EMC and ESD handling capability. Improved slope control and high DC handling capability on the bus pins provides additional application flexibility.

The TJA1051 is available in two versions, distinguished only by the function of pin 5:

- The TJA1051T is 100 % backwards compatible with the TJA1050
- The TJA1051T/3 and TJA1051TK/3 allow for direct interfacing to microcontrollers with supply voltages down to 3 V

6.1 Operating modes

The TJA1051 supports two operating modes, Normal and Silent, which are selectable via pin S. See Table 3 for a description of the operating modes under normal supply conditions.

Table 3. Operating modes

Mode	Inputs		Outputs	
	Pin S	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	active[1]
	LOW	HIGH	recessive	active[1]
Silent	HIGH	X[2]	recessive	active[1]

[1] LOW if the CAN bus is dominant, HIGH if the CAN bus is recessive.

[2] X = don't care

6.1.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver is able to transmit and receive data via the bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible ElectroMagnetic Emission (EME).

6.1.2 Silent mode

A HIGH level on pin S selects Silent mode. In Silent mode the transmitter is disabled, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

6.2 Fail-safe features

6.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

6.2.2 Internal biasing of TXD and S input pins

Pin TXD has an internal pull-up to V_{IO} and pin S has an internal pull-down to GND. This ensures a safe, defined state in case one or both of these pins are left floating.

6.2.3 Undervoltage detection on pins V_{CC} and V_{IO}

Should V_{CC} or V_{IO} drop below their respective undervoltage detection levels ($V_{uvd(VCC)}$ and $V_{uvd\ (VIO)}$; see Table 6), the transceiver will switch off and disengage from the bus (zero load) until V_{CC} and V_{IO} have recovered.

6.2.4 Over-temperature protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the output drivers will be disabled until the virtual junction temperature falls below $T_{j(sd)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillations due to temperature drift are avoided.

6.3 V_{IO} supply pin

Two versions of the TJA1051 are available, only differing in the function of a single pin. Pin 5 is either not connected or is a V_{IO} supply pin.

Pin V_{IO} on the TJA1051T/3 and TJA1051TK/3 should be connected to the microcontroller supply voltage (see Figure 3). This will adjust the signal levels of pins TXD, RXD and S to the I/O levels of the microcontroller. For versions of the TJA1051 without a V_{IO} pin, the V_{IO} input is internally connected to V_{CC}. This sets the signal levels of pins TXD, RXD and S to levels compatible with 5 V microcontrollers.

7. Application design-in information

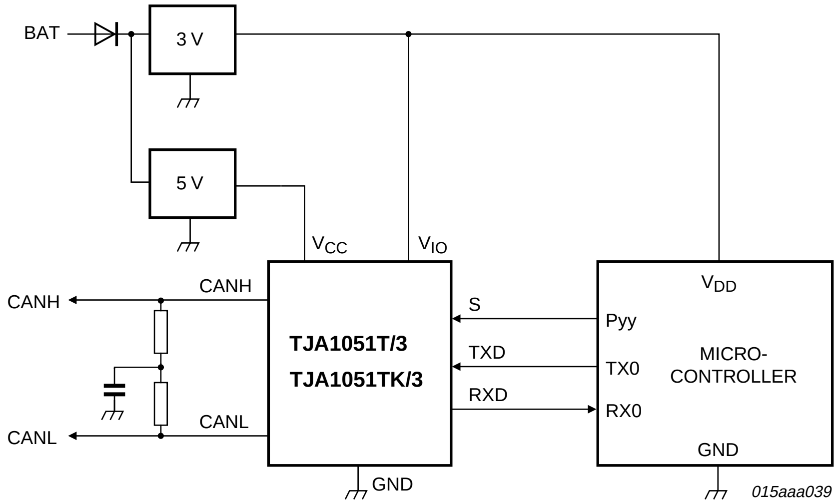


Fig 3. Typical application of the TJA1051T/3 or TJA1051TK/3.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_x	voltage on pin x	no time limit; DC value				
		on pins CANH and CANL		–58	+58	V
		on any other pin		–0.3	+7	V
V_{trt}	transient voltage	on pins CANH and CANL	[1]	–150	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2	[2]			
		at pins CANH and CANL	[3]	–8	+8	kV
		HBM	[4]			
		at pins CANH and CANL		–8	+8	kV
		at any other pin		–4	+4	kV
		MM	[5]			
		at any pin		–300	+300	V
		CDM	[6]			
		at corner pins		–750	+750	V
		at any pin		–500	+500	V
T_{vj}	virtual junction temperature		[7]	–40	+150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+125	°C

[1] Verified by an external test house to ensure pins CANH and CANL can withstand ISO 7637 part 3 automotive transient test pulses 1, 2a, 3a and 3b.

[2] IEC 61000-4-2 (150 pF, 330 Ω).

[3] ESD performance of pins CANH and CANL according to IEC 61000-4-2 (150 pF, 330 Ω) has been be verified by an external test house. The result is equal to or better than ±8 kV (unaided).

[4] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[5] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 μH, 10 Ω).

[6] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF). The classification level is C5 (> 1000 V).

[7] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 5. Thermal characteristics

According to IEC 60747-1.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient	SO8 package; in free air	155	K/W
		HVSON8 package; in free air	55	K/W

10. Static characteristics

Table 6. Static characteristics

T_{vj} = −40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V[1]; R_L = 60 Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC[2].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Silent mode	0.1	1	2.5	mA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$	2.5	5	10	mA
		dominant; V_{TXD} = 0 V	20	50	70	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.5	V
I/O level adapter supply; pin V_{IO}[1]						
V_{IO}	supply voltage on pin V_{IO}		2.8	-	5.5	V
I_{IO}	supply current on pin V_{IO}	Normal and Silent modes				
		recessive; $V_{TXD} = V_{IO}$	10	80	250	μA
		dominant; V_{TXD} = 0 V	50	350	500	μA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	-	2.7	V
Mode control input; pin S						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	$V_{IO} + 0.3$	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	$V_S = V_{IO}$	1	4	10	μA
I_{IL}	LOW-level input current	V_S = 0 V	−1	0	+1	μA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	$V_{IO} + 0.3$	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V

Table 6. Static characteristics *...continued*

T_{vj} = –40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V[1]; R_L = 60 Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC[2].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	$V_{TXD} = V_{IO}$		–5	0	+5	µA
I_{IL}	LOW-level input current	Normal mode; V_{TXD} = 0 V		–260	–150	–30	µA
C_i	input capacitance		[3]	-	5	10	pF
CAN receive data output; pin RXD							
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$ – 0.4 V; $V_{IO} = V_{CC}$		–8	–3	–1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant		2	5	12	mA
Bus lines; pins CANH and CANL							
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$					
		pin CANH		2.75	3.5	4.5	V
		pin CANL		0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$		–400	0	+400	mV
$V_{O(dif)bus}$	bus differential output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$ R_L = 45 Ω to 65 Ω		1.5	-	3	V
		$V_{TXD} = V_{IO}$; recessive; no load		–50	-	+50	mV
$V_{O(rec)}$	recessive output voltage	Normal and Silent modes; $V_{TXD} = V_{IO}$; no load		2	$0.5V_{CC}$	3	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal and Silent modes $V_{cm(CAN)}$[4] = –30 V to +30 V		0.5	0.7	0.9	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal and Silent modes $V_{cm(CAN)}$ = –30 V to +30 V		50	120	200	mV
$I_{O(dom)}$	dominant output current	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 5 V					
		pin CANH; V_{CANH} = 0 V		–100	–70	–40	mA
		pin CANL; V_{CANL} = 5 V / 40 V		40	70	100	mA
$I_{O(rec)}$	recessive output current	Normal and Silent modes; $V_{TXD} = V_{IO}$ $V_{CANH} = V_{CANL}$ = –27 V to +32 V		–5	-	+5	mA
I_L	leakage current	$V_{CC} = V_{IO}$ = 0 V; $V_{CANH} = V_{CANL}$ = 5 V		–5	0	+5	µA
R_i	input resistance			9	15	28	kΩ
ΔR_i	input resistance deviation	between V_{CANH} and V_{CANL}		–1	0	+1	%
$R_{i(dif)}$	differential input resistance			19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance		[3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance		[3]	-	-	10	pF
Temperature protection							
$T_{j(sd)}$	shutdown junction temperature		[3]	-	190	-	°C

[1] Only TJA1051T/3 and TJA1051TK/3 have a V_{IO} pin. In transceivers without a V_{IO} pin, the V_{IO} input is internally connected to V_{CC}.

[2] All parameters are guaranteed over the virtual junction temperature range by design. Products are 100 % tested at 125 °C ambient temperature (wafer level pretesting), and 100 % tested at 25 °C ambient temperature (final testing). Both pretesting and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.

[3] Not tested in production.

[4] $V_{cm(CAN)}$ is the common mode voltage of CANH and CANL.

11. Dynamic characteristics

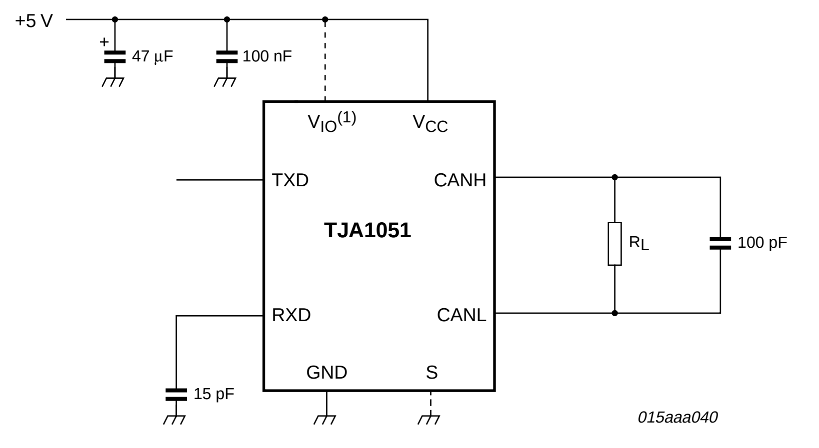
Table 7. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to 5.5 V[1]; R_L = 60 Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 4 and Figure 5						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	65	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	90	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal and Silent modes	-	60	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal and Silent modes	-	65	-	ns
$t_{PD(TXD-RXD)}$	propagation delay from TXD to RXD	versions with pin 5 n.c. Normal mode	40	-	220	ns
		versions with V_{IO} pin Normal mode	40	-	250	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode	0.3	1	12	ms

[1] Only TJA1051T/3 and TJA1051TK/3 have a V_{IO} pin. In transceivers without a V_{IO} pin, the V_{IO} input is internally connected to V_{CC}.

[2] All parameters are guaranteed over the virtual junction temperature range by design. Products are 100 % tested at 125 °C ambient temperature (wafer level pretesting), and 100 % tested at 25 °C ambient temperature (final testing). Both pretesting and final testing use correlated test conditions to cover the specified temperature and power supply voltage range.



(1) For versions with a V_{IO} pin (TJA1051T/3 and TJA1051TK/3), the V_{IO} input is connected to pin V_{CC}.

Fig 4. Timing test circuit for CAN transceiver

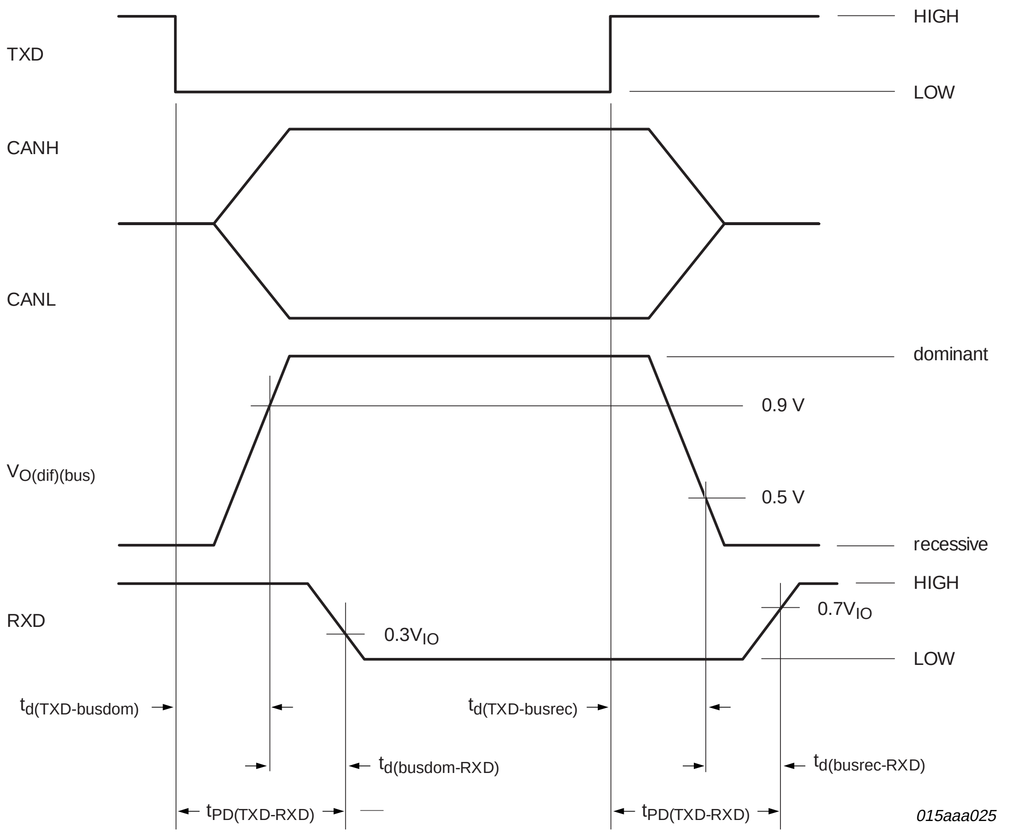


Fig 5. CAN transceiver timing diagram

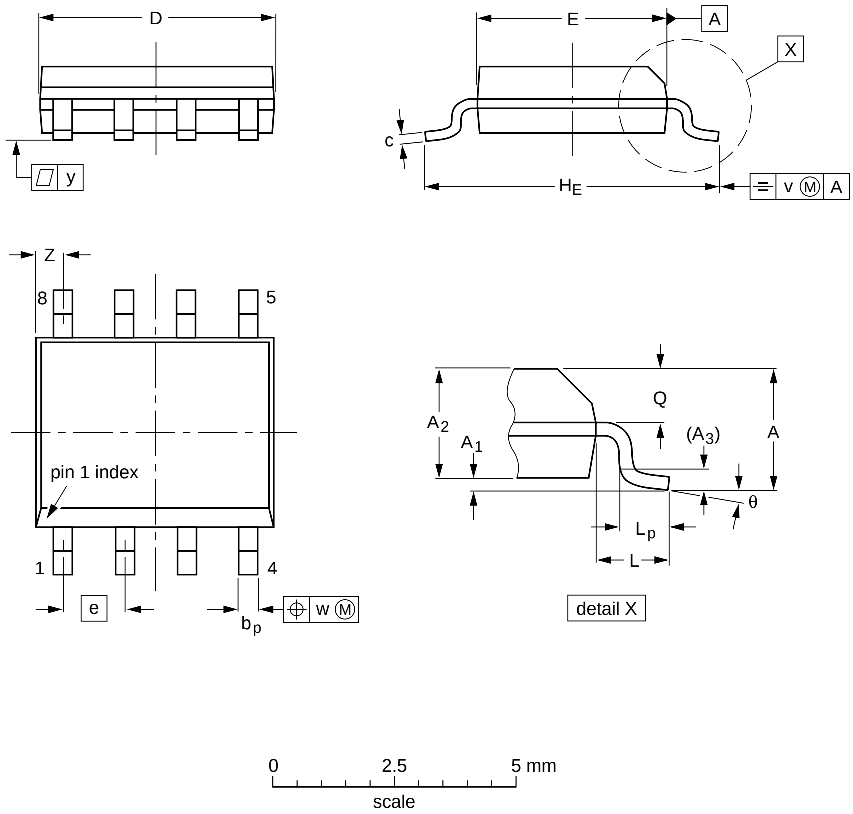
12. Test information

12.1 Quality information

This product has been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 or Q101 and is suitable for use in automotive applications.

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

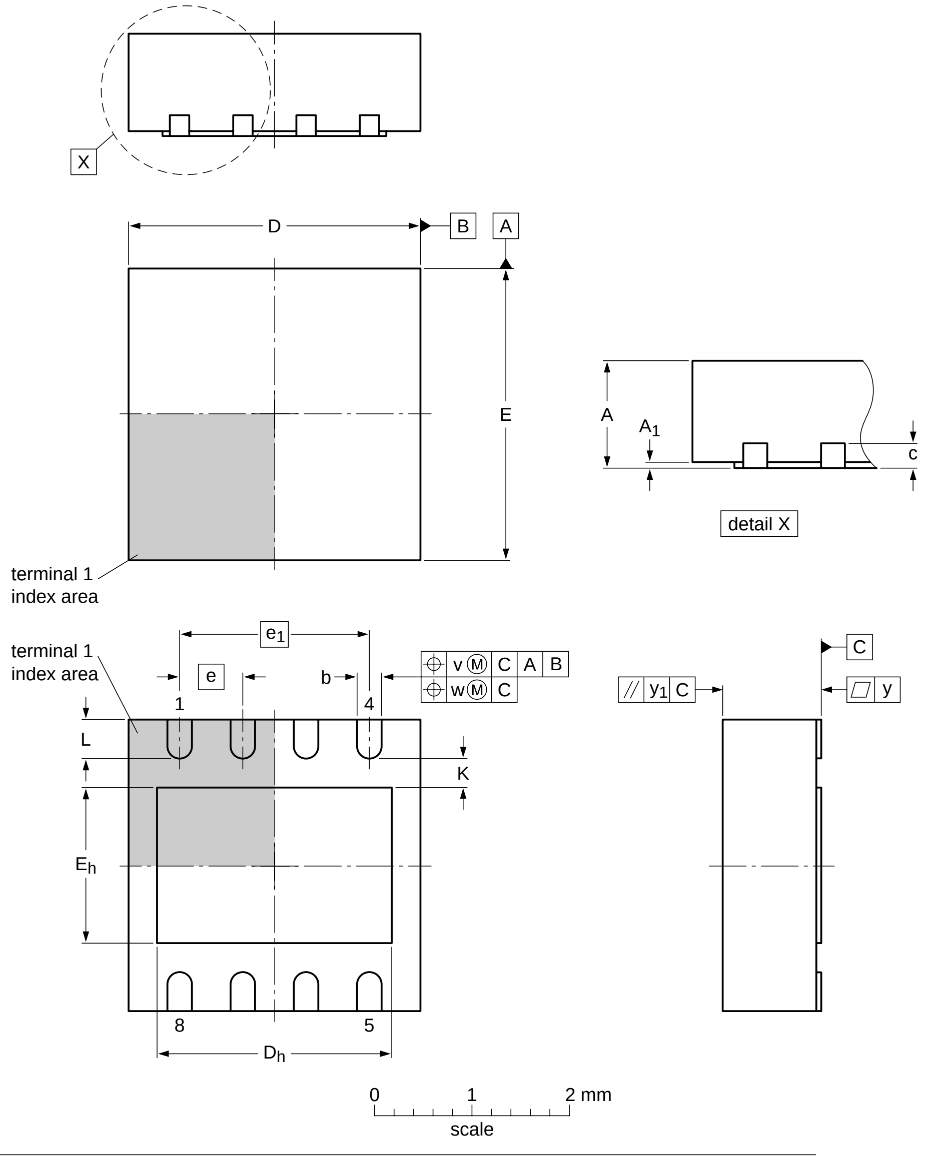
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 6. Package outline SOT96-1 (SO8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT782-1**



Dimensions

Unit[1]		A	A_1	b	c	D	D_h	E	E_h	e	e_1	K	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		3.10	2.45	3.10	1.65			0.35	0.45				
	nom	0.85	0.03	0.30	0.2	3.00	2.40	3.00	1.60	0.65	1.95	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		2.90	2.35	2.90	1.55			0.25	0.35				

Note

1. Plastic or metal protrusions of 0.075 maximum per side are not included.

sot782-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT782-1	- - -	MO-229	- - -			~~09-08-25~~ 09-08-28

Fig 7. Package outline SOT782-1 (HVSON8)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020C)

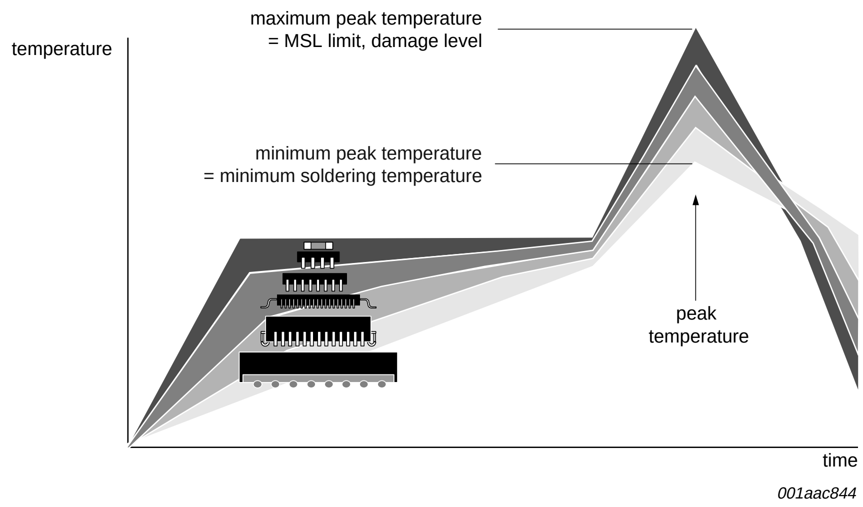
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.



MSL: Moisture Sensitivity Level

Fig 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1051_4	20091020	Product data sheet	-	TJA1051_3
Modifications • Revised parameter values in Table 4 (V_{ESD})				
TJA1051_3	20090825	Product data sheet	-	TJA1051_2
TJA1051_2	20090701	Product data sheet	-	TJA1051_1
TJA1051_1	20090309	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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