

# MC14583B

## Dual Schmitt Trigger

The MC14583B is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Resistor Adjustable Trigger Levels

### MAXIMUM RATINGS\* (Voltages Referenced to V<sub>SS</sub>)

| Symbol                             | Parameter  | Value                          | Unit |
|------------------------------------|--|--------------------------------|------|
| V <sub>DD</sub>                    | DC Supply Voltage                                  | - 0.5 to + 18.0                | V    |
| V <sub>in</sub> , V <sub>out</sub> | Input or Output Voltage (DC or Transient)          | - 0.5 to V <sub>DD</sub> + 0.5 | V    |
| I <sub>in</sub> , I <sub>out</sub> | Input or Output Current (DC or Transient), per Pin | ± 10                           | mA   |
| P <sub>D</sub>                     | Power Dissipation, per Package†                    | 500                            | mW   |
| T <sub>stg</sub>                   | Storage Temperature                                | - 65 to + 150                  | °C   |
| T <sub>L</sub>                     | Lead Temperature (8-Second Soldering)              | 260                            | °C   |

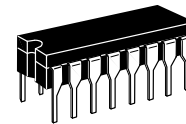
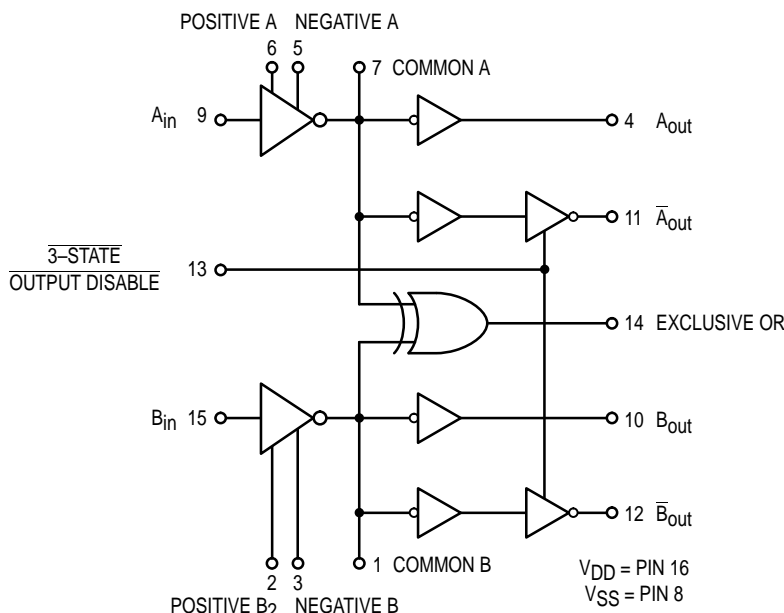
\* Maximum Ratings are those values beyond which damage to the device may occur.

† Temperature Derating:

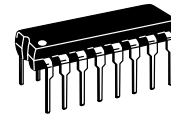
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

Ceramic "L" Packages: - 12 mW/°C From 100°C To 125°C

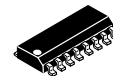
### LOGIC DIAGRAM



**L SUFFIX**  
CERAMIC  
CASE 620



**P SUFFIX**  
PLASTIC  
CASE 648



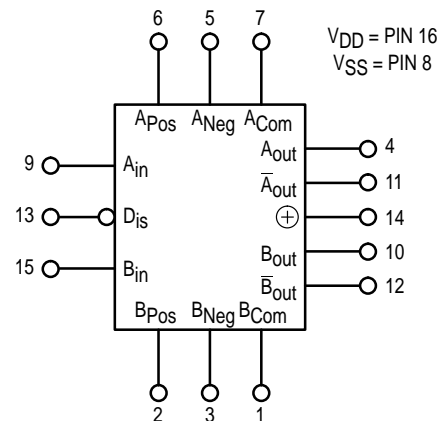
**D SUFFIX**  
SOIC  
CASE 751B

### ORDERING INFORMATION

MC14XXXBCP    Plastic  
MC14XXXBCL    Ceramic  
MC14XXXBD    SOIC

T<sub>A</sub> = - 55° to 125°C for all packages.

### BLOCK DIAGRAM



### TRUTH TABLE

| Inputs |   |     | Outputs          |                    |                  |                    |   |
|--------|---|-----|------------------|--------------------|------------------|--------------------|---|
| A      | B | Dis | A <sub>out</sub> | A <sub>out</sub> ̄ | B <sub>out</sub> | B <sub>out</sub> ̄ | ⊕ |
| 0      | 0 | 0   | 0                | Z                  | 0                | Z                  | 0 |
| 0      | 0 | 1   | 0                | 1                  | 0                | 1                  | 0 |
| 0      | 1 | 0   | 0                | Z                  | 1                | Z                  | 1 |
| 0      | 1 | 1   | 0                | 1                  | 1                | 0                  | 1 |
| 1      | 0 | 0   | 1                | Z                  | 0                | Z                  | 1 |
| 1      | 0 | 1   | 1                | 0                  | 0                | 1                  | 1 |
| 1      | 1 | 0   | 1                | Z                  | 1                | Z                  | 0 |
| 1      | 1 | 1   | 1                | 0                  | 1                | 0                  | 0 |

Z = High impedance at output

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

| Characteristic  | Symbol  | V <sub>DD</sub><br>Vdc | - 55°C   |       | 25°C  |          |       | 125°C  |       | Unit |   |
|---|---|------------------------|--|-------|-------|----------|-------|--------|-------|------|---|
|   |   |                        | Min  | Max   | Min   | Typ #    | Max   | Min    | Max   |      |   |
| Output Voltage<br>V <sub>in</sub> = V <sub>DD</sub> or 0  | "0" Level<br>V <sub>OL</sub>  | 5.0                    | —  | 0.05  | —     | 0        | 0.05  | —      | 0.05  | Vdc  |   |
|   |   | 10                     | —  | 0.05  | —     | 0        | 0.05  | —      | 0.05  |      |   |
|   |   | 15                     | —  | 0.05  | —     | 0        | 0.05  | —      | 0.05  |      |   |
|   | "1" Level<br>V <sub>in</sub> = 0 or V <sub>DD</sub>   | V <sub>OH</sub>        | 5.0  | 4.95  | —     | 4.95     | 5.0   | —      | 4.95  |      | — |
|   |   |                        | 10   | 9.95  | —     | 9.95     | 10    | —      | 9.95  |      | — |
|   |   |                        | 15   | 14.95 | —     | 14.95    | 15    | —      | 14.95 |      | — |
| Input Voltage<br>(V <sub>O</sub> = 4.5 or 0.5 Vdc)<br>(V <sub>O</sub> = 9.0 or 1.0 Vdc)<br>(V <sub>O</sub> = 13.5 or 1.5 Vdc)                     | "0" Level<br>V <sub>IL</sub>  | 5.0                    | —  | 1.5   | —     | 2.25     | 1.5   | —      | 1.5   | Vdc  |   |
|   |   | 10                     | —  | 3.0   | —     | 4.50     | 3.0   | —      | 3.0   |      |   |
|   |   | 15                     | —  | 4.0   | —     | 6.75     | 4.0   | —      | 4.0   |      |   |
|   | "1" Level<br>(V <sub>O</sub> = 0.5 or 4.5 Vdc)<br>(V <sub>O</sub> = 1.0 or 9.0 Vdc)<br>(V <sub>O</sub> = 1.5 or 13.5 Vdc) | V <sub>IH</sub>        | 5.0  | 3.5   | —     | 3.5      | 2.75  | —      | 3.5   |      | — |
|   |   |                        | 10   | 7.0   | —     | 7.0      | 5.50  | —      | 7.0   |      | — |
|   |   |                        | 15   | 11    | —     | 11       | 8.25  | —      | 11    |      | — |
| Output Drive Current<br>(V <sub>OH</sub> = 2.5 Vdc)<br>(V <sub>OH</sub> = 4.6 Vdc)<br>(V <sub>OH</sub> = 9.5 Vdc)<br>(V <sub>OH</sub> = 13.5 Vdc) | Source<br>I <sub>OH</sub>   | 5.0                    | - 1.2  | —     | - 1.0 | - 1.7    | —     | - 0.7  | —     | mAdc |   |
|   |   | 5.0                    | - 0.25   | —     | - 0.2 | - 0.36   | —     | - 0.14 | —     |      |   |
|   |   | 10                     | - 1.62   | —     | - 0.5 | - 0.9    | —     | - 0.35 | —     |      |   |
|   | 15  | - 1.8                  | —  | - 1.5 | - 3.5 | —        | - 1.1 | —      |       |      |   |
|   | Sink<br>I <sub>OL</sub>   | 5.0                    | 0.64   | —     | 0.51  | 0.88     | —     | 0.36   | —     |      |   |
|   |   | 10                     | 1.6  | —     | 1.3   | 2.25     | —     | 0.9    | —     |      |   |
| 15  |   | 4.2                    | —  | 3.4   | 8.8   | —        | 2.4   | —      |       |      |   |
| Input Current   | I <sub>in</sub>   | 15                     | —  | ±0.1  | —     | ±0.00001 | ±0.1  | —      | ±1.0  | μAdc |   |
| Input Capacitance<br>(V <sub>in</sub> = 0)  | C <sub>in</sub>   | —                      | —  | —     | —     | 5.0      | 7.5   | —      | —     | pF   |   |
| Quiescent Current<br>(Per Package)  | I <sub>DD</sub>   | 5.0                    | —  | 0.25  | —     | 0.0005   | 0.25  | —      | 7.5   | μAdc |   |
|   |   | 10                     | —  | 0.5   | —     | 0.0010   | 0.5   | —      | 15    |      |   |
|   |   | 15                     | —  | 1.0   | —     | 0.0015   | 1.0   | —      | 30    |      |   |
| Total Supply Current**†<br>(Dynamic plus Quiescent,<br>Per Package)<br>(C <sub>L</sub> = 50 pF on all outputs, all<br>buffers switching)          | I <sub>T</sub>  | 5.0                    | I <sub>T</sub> = (1.33 μA/kHz) f + I <sub>DD</sub> |       |       |          |       |        |       | μAdc |   |
|   |   | 10                     | I <sub>T</sub> = (2.65 μA/kHz) f + I <sub>DD</sub> |       |       |          |       |        |       |      |   |
|   |   | 15                     | I <sub>T</sub> = (3.98 μA/kHz) f + I <sub>DD</sub> |       |       |          |       |        |       |      |   |
| Three-State Leakage Current   | I <sub>TL</sub>   | 15                     | —  | ±0.1  | —     | ±0.0001  | ±0.1  | —      | ±3.0  | μAdc |   |

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

\*\*The formulas given are for the typical characteristics only at 25°C.

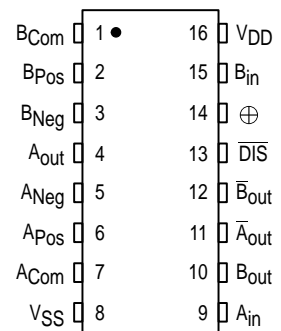
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.005.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

**PIN ASSIGNMENT**

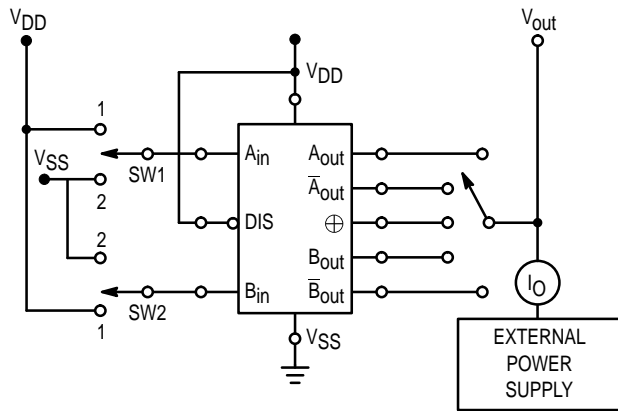


**SWITCHING CHARACTERISTICS\*** ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

| Characteristic   | Symbol                  | V <sub>DD</sub> | Min                  | Typ #                | Max                  | Unit |
|--|-------------------------|-----------------|----------------------|----------------------|----------------------|------|
| Output Rise Time<br>$t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$<br>$t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$<br>$t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$  | $t_{TLH}$               | 5.0<br>10<br>15 | —<br>—<br>—          | 180<br>90<br>65      | 360<br>180<br>130    | ns   |
| Output Fall Time<br>$t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$<br>$t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$<br>$t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$   | $t_{THL}$               | 5.0<br>10<br>15 | —<br>—<br>—          | 100<br>50<br>40      | 200<br>100<br>80     | ns   |
| Propagation Delay Time<br>$A_{in}, B_{in}$ to $A_{out}, B_{out}$<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 565 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$ | $t_{PLH},$<br>$t_{PHL}$ | 5.0<br>10<br>15 | —<br>—<br>—          | 650<br>230<br>150    | 1300<br>460<br>300   | ns   |
| $A_{in}, B_{in}$ to $A_{out}, B_{out}$<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 1015 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 347 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 235 \text{ ns}$                          | $t_{PLH},$<br>$t_{PHL}$ | 5.0<br>10<br>15 | —<br>—<br>—          | 1100<br>380<br>260   | 2200<br>760<br>520   | ns   |
| $A_{in}, B_{in}$ to Exclusive OR<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 665 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 257 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 145 \text{ ns}$                                 | $t_{PLH},$<br>$t_{PHL}$ | 5.0<br>10<br>15 | —<br>—<br>—          | 750<br>280<br>170    | 1500<br>560<br>340   | ns   |
| 3-State Enable, Disable Delay Time (see figure 5)<br>$t_{on}, t_{off} = (1.7 \text{ ns/pF}) C_L + 140 \text{ ns}$<br>$t_{on}, t_{off} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$<br>$t_{on}, t_{off} = (0.5 \text{ ns/pF}) C_L + 30 \text{ ns}$                     | $t_{on},$<br>$t_{off}$  | 5.0<br>10<br>15 | —<br>—<br>—          | 225<br>90<br>55      | 450<br>180<br>110    | ns   |
| Positive Threshold Voltage<br>(R1, R2 = 5.0 k $\Omega$ )   | $V_{T+}$                | 5.0<br>10<br>15 | —<br>—<br>—          | 3.30<br>5.70<br>8.20 | —<br>—<br>—          | Vdc  |
| Negative Threshold Voltage<br>(R1, R2 = 5.0 k $\Omega$ )   | $V_{T-}$                | 5.0<br>10<br>15 | —<br>—<br>—          | 1.70<br>4.30<br>6.80 | —<br>—<br>—          | Vdc  |
| Hysteresis Voltage<br>(R1, R2 = 5.0 k $\Omega$ )   | $V_H$                   | 5.0<br>10<br>15 | 0.85<br>0.70<br>0.70 | 1.70<br>1.40<br>1.40 | 3.40<br>2.80<br>2.80 | Vdc  |
| Threshold Voltage Variation, A to B<br>(R1, R2 = 5.0 k $\Omega$ )  | $\Delta V_T$            | 5.0<br>10<br>15 | —<br>—<br>—          | 0.1<br>0.15<br>0.20  | —<br>—<br>—          | Vdc  |

\* The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



| Output Under Test                   | Output Source Characteristics  |     | Output Sink Characteristics  |     |
|-------------------------------------|--|-----|--|-----|
|                                     | Test Value $\begin{cases} V_{GS} = -V_{DD} \\ V_{DS} = V_{out} - V_{DD} \end{cases}$ |     | Test Value $\begin{cases} V_{GS} = V_{DD} \\ V_{DS} = V_{out} \end{cases}$ |     |
|                                     | Switch Position  |     | Switch Position  |     |
|                                     | SW1  | SW2 | SW1  | SW2 |
| A <sub>out</sub> , B <sub>out</sub> | 1  | 1   | 2  | 2   |
| $\bar{A}_{out}$ , $\bar{B}_{out}$   | 2  | 2   | 1  | 1   |
| Exclusive OR                        | 1  | 2   | 1  | 1   |

Figure 1. Typical Output Source and Sink Characteristics Test Circuit

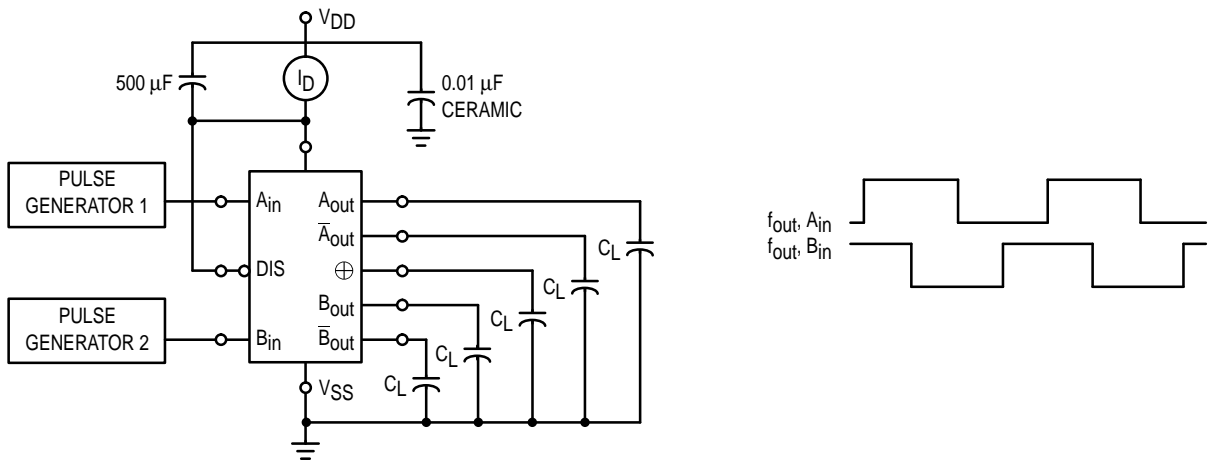
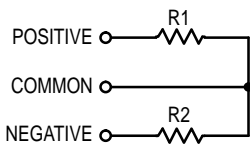


Figure 2. Power Dissipation Test Circuit and Waveforms

A — Feedback scheme for independent threshold adjustment:



B — Feedback scheme for hysteresis adjustment:

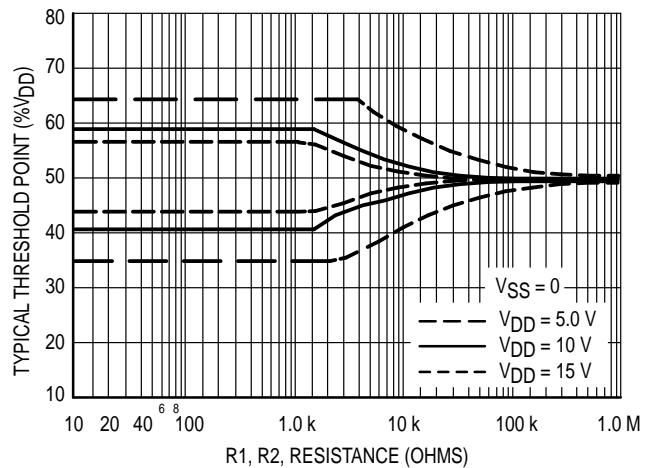
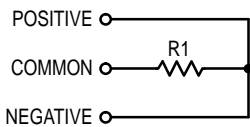
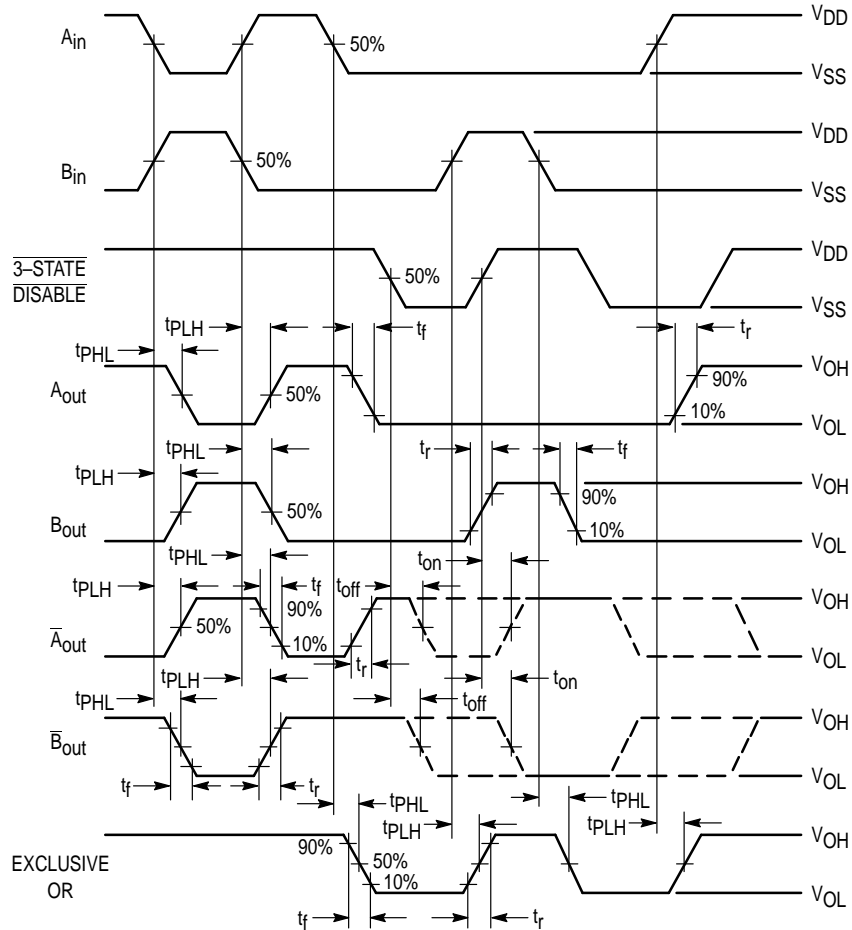
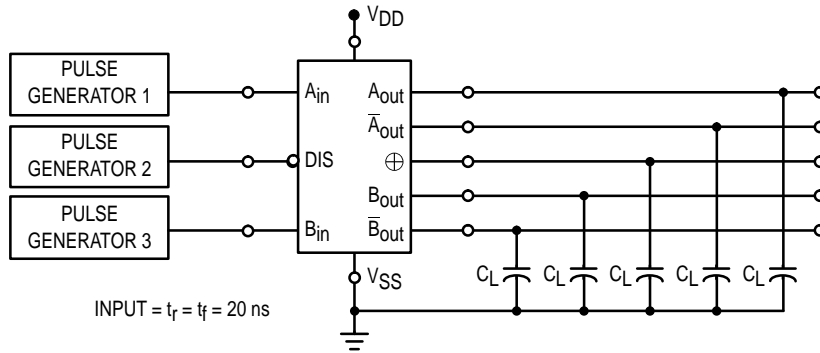
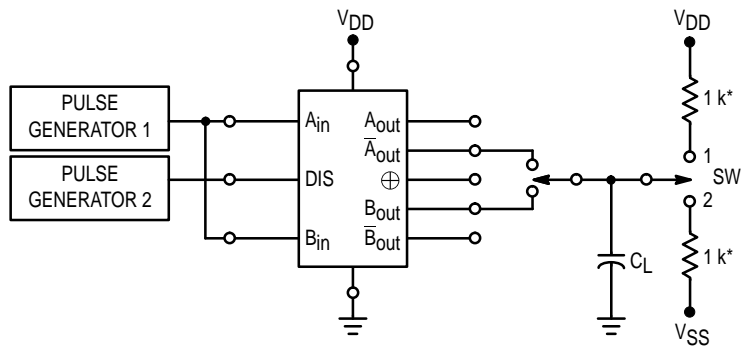


Figure 3. Typical Threshold Points



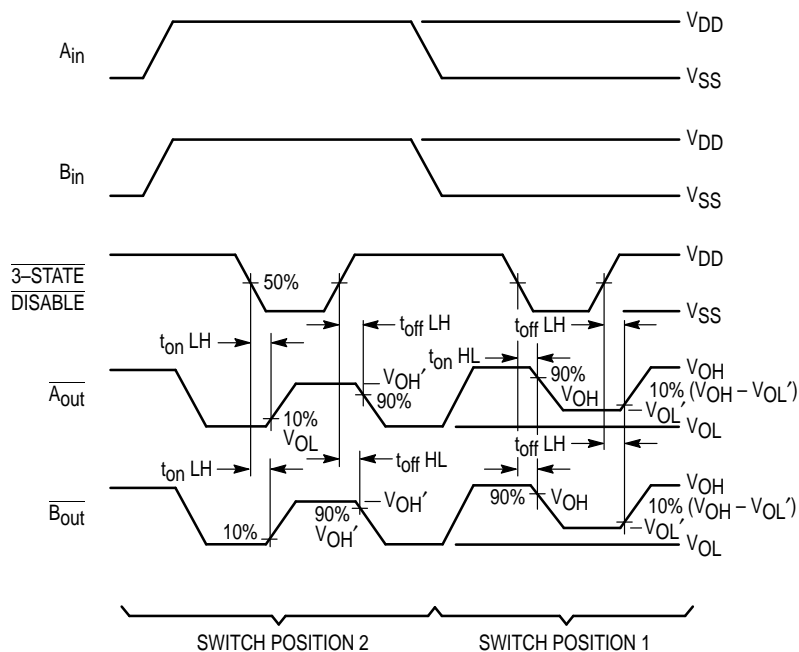
NOTE: Dashed lines indicate high output resistance

**Figure 4. Switching Time Test Circuit and Waveforms**



| Test          | Switch Position |
|---------------|-----------------|
| $t_{on\ HL}$  | 1               |
| $t_{on\ LH}$  | 2               |
| $t_{off\ HL}$ | 2               |
| $t_{off\ LH}$ | 1               |

\* Metal film,  $\pm 1\%$ , 1/4 W or greater  
 $C_L = 15\text{ pF}$ , which includes test circuit capacitance.

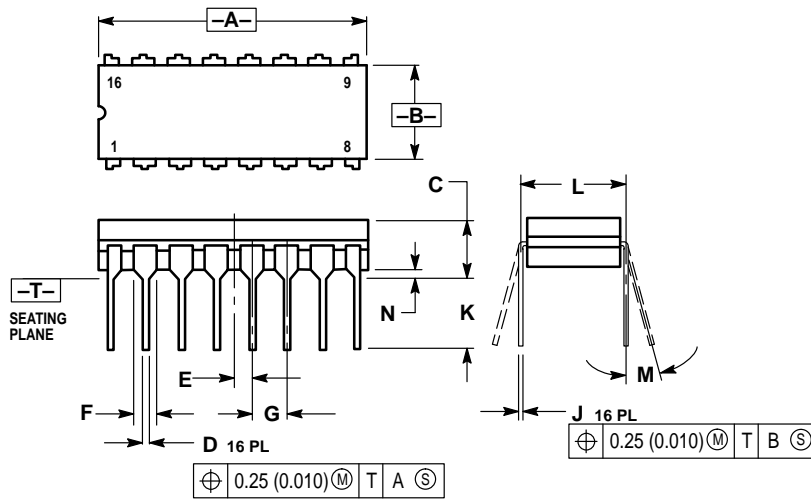


$V_{OL}'$  and  $V_{OH}'$  refer to the levels present as a result of the 1 k ohm load resistors.

**Figure 5. 3-State Switching Time Test Circuit and Waveforms**

## OUTLINE DIMENSIONS

### L SUFFIX CERAMIC DIP PACKAGE CASE 620-10 ISSUE V

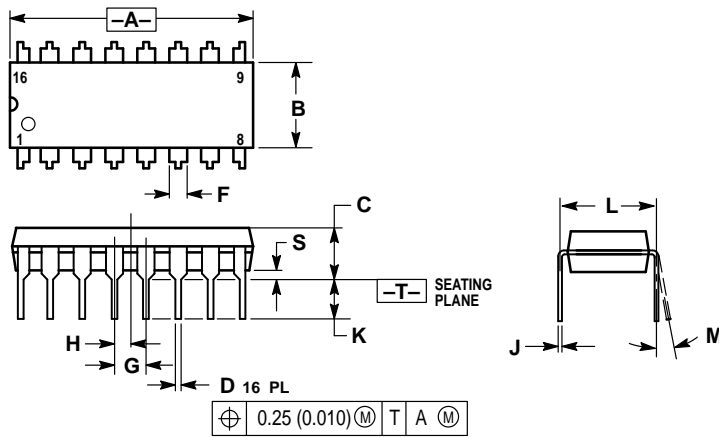


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.750     | 0.785 | 19.05       | 19.93 |
| B   | 0.240     | 0.295 | 6.10        | 7.49  |
| C   | —         | 0.200 | —           | 5.08  |
| D   | 0.015     | 0.020 | 0.39        | 0.50  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.055     | 0.065 | 1.40        | 1.65  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.125     | 0.170 | 3.18        | 4.31  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0°        | 15°   | 0°          | 15°   |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |

### P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



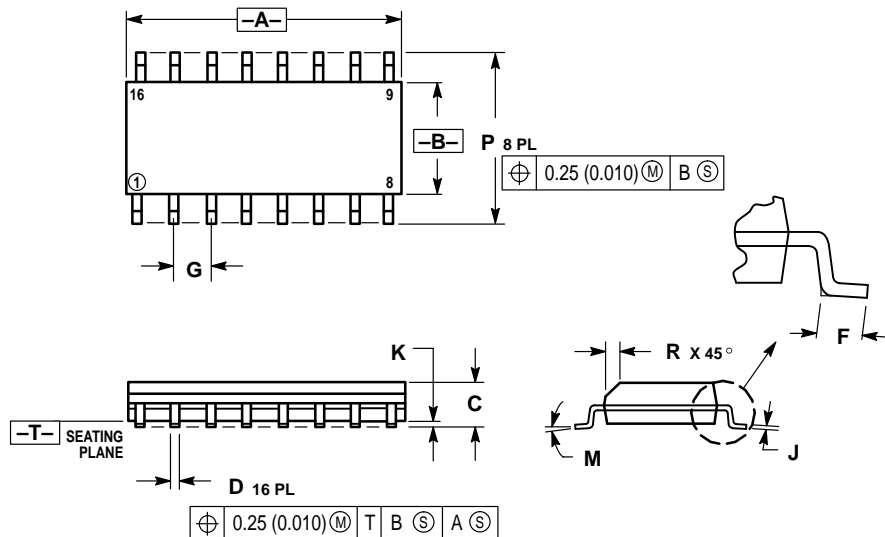
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

## OUTLINE DIMENSIONS

### D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

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